CLAIMS

1. A transistor including at least one narrow bandgap region or layer that is doped p-type or contains an excess of holes and is subject to compressive mechanical strain.

2. A transistor according to claim 1 wherein said narrow bandgap region or layer is arranged for majority carrier transport.

3. A transistor according to claim 1 or claim 2 wherein said narrow bandgap region or layer is in contact with at least one further region or layer having a different lattice constant whereby said narrow bandgap region or layer is subject to said compressive mechanical strain.

4. A transistor according to any preceding claim wherein there are at least two said further layers, one on each side of said narrow bandgap region or layer.

5. A transistor according to any preceding claim wherein said narrow bandgap region or layer comprises InSb or InAs.

6. A transistor according to any preceding claim wherein the transistor is a quantum-well FET.

7. A transistor according to claim 6 wherein the quantum well is provided by a primary conduction channel and at least one secondary conduction channel immediately adjacent and in contact with the primary channel, the secondary channel having an effective bandgap greater than the effective bandgap Eg (effective) of the primary channel, wherein the modulus of the difference between the effective impact ionisation threshold IIT (effective) and the effective conduction band offset $\Delta E_C$ (effective) between the primary and secondary channels being no more than 0.5 Eg (effective).

8. A transistor according to claim 7 wherein the quantum well is provided by a primary conduction channel and at least one secondary conduction channel immediately adjacent and in contact with the primary channel, the secondary channel

having an effective bandgap greater than the effective bandgap Eg (effective) of the primary channel, wherein the modulus of the difference between the effective impact ionisation threshold IIT (effective) and the effective conduction band offset $\Delta E_C$ (effective) between the primary and secondary channels being no more than 0.4 eV.

9. A transistor according to claim 6 in the form of an extracting transistor characterised in that (a) it is a field effect transistor incorporating a conducting region consisting at least partly of a quantum well; (b) the quantum well is in an at least partly intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature; and (c) it includes at least one junction which is biasable to reduce the intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime.

10. A transistor according to any one of claims 1 to 5 wherein the transistor is an n-p-n bipolar transistor.

11. A transistor according to claim 10 with a vertical geometry having a base region provided with a base contact, emitter and collector regions arranged to extract minority carriers from the base region, and a structure for counteracting entry of minority carriers into the base region via the base contact, wherein the base region has a bandgap of greater than 0.5 eV and a doping level greater than $10^{17}$ $cm^{-3}$.

12. A transistor according to any preceding claim wherein the narrow bandgap is no more than 1.0 eV.

13. Complementary logic circuitry comprising a transistor according to any preceding claim.

14. An integrated circuit comprising a transistor according to any one of claims 1 to 12 or complementary logic circuitry according to claim 13.

15. A transistor substantially as hereinbefore described with reference to Figure 1 or Figure 4 of the accompanying drawings.